media and signal decay, the correct sampling of data streams still depends on the correct clock pulse. In addition, the rising/falling edges of the clock pulses need to be in the middle of the data period to sample them correctly. The conventional data recovery system uses a phase-lock loop circuit to achieve the

5   clock-recovery in order to correct the received data stream and sampling clock pulses. However, several disadvantages exist when the phase-lock loop circuit is used for recovering the clock-pulse, including: (a) Longer lock time. The function of the phase-lock loop circuit rectifying the phase is to use the output signal reference frequency and the voltage-controlled oscillator to compare with each

10   other and transfer the result to the voltage signal. The feedback of the input of the voltage-controlled oscillator rectifies the frequency in order to accelerate or slow down the phase. The process of the rectification of the phase has to compare many clock-pulse cycles with each other in order to achieve the phase needed. Maybe several hundreds of the clock-pulse cycles are needed for the

15   comparison. As a result, longer lock-time is required. (b) Phase noise. The input voltage of the voltage-controlled oscillator of the phase-lock loop circuit will lead the frequency drift when the noise disturbs. The result above is the phase noise. When clock-pulse is recovering, comparison of phases also depends on sequence of the received data stream. Because the rising and falling edges of

20   the signal do not vary when a long and same logical signal inputs, the phase detector won't work. Under such condition, the phase-lock loop circuit is unable to maintain the phase-lock state and the frequency will start to drift, and, as a

result, the phase noise is generated in the frequency spectrum. (c) Only one

receiving channel is available. Only one receiving channel can be provided when

we achieve the clock-pulse recovery by using the phase-lock loop circuit. We

have to recover the clock-pulse by using more phase-lock loop circuits for a

5   plurality of receiving channels.

[0004]   Therefore, multiphase systems have become a trend for data-recovery

systems during the recent years. Since multi-phases may be distributed in one

clock-pulse, the above mentioned phase-lock process can be achieved by

selecting a suitable sampling clock-pulse. Not only phase-lock time is shorter, we

10   can also provide a phase-lock loop circuit for use with a plurality of receiving

channels. There are several methods to generate multiphase signals, including:

(a) Delay-Lock loop. Using a long series of delay chain, such as two inverters

connected in serial, to generate clock-pulse signals having different delay

duration so as to form the multiphase signals. The advantage for this method is

15   the stability. However, it also incurs the drawbacks of requiring lots of delay units

for covering 360 degrees of clock-pulse phases, higher cost, fewer applications

available, more electric power decay, and inevitable noise disturbance occurred

from electrical power lines. (b) Multiphase VCO. Currently, the newly developed

multiphase oscillators are able to generate refined differences of phases

20   uniformly distributed within one clock-pulse. In addition, the number of the

generated multiphase signals can be the power of two. However, one of the

difficulties is to avoid the problem of the multiphase oscillator model. The circuit

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layout is also an important consideration for this method. (c) The phase

interpolation. The phase interpolation is one of the ways to generate the

multiphase signals. A middle phase can be output by inputting different phases.

The way to use the phase interpolation is easier and is the trend for future

5   technology.

[0005]   The advantages of the phase interpolation in comparison with the above

mentioned conventional techniques are following: (a) It won't be limited by the

delay time of the delay unit to decide the distribution density of the multiphase.

The multiphase density and number can be easily decided by phase interpolation.

10   The cost and the decaying power will balance in the design. The system is also

very stable. (b) There is no disadvantage of the multi-oscillating model. And the

number of the phases will increase by doubling the number of the input phase

after the interpolation. For example, we can interpolate 8 phases once if we need

16 phases. (8*2=16) If we need 20 phases then we can interpolate 10 phases

15   once. (10*2=20) Or, to interpolate 5 phases twice can also obtain the same result.

The design is very free. (c) Because the phase-interpolation can produce the

local multiphase clock signals by using fewer phases of the globe clock signals,

therefore the area of the wiring and the number of the clock-pulse buffers will be

fewer than the decay-lock-loop circuit and the multiphase oscillator in the

20   application of the multi-receiving channels.

[0006]   Conventional phase-interpolation methods include the type of non-full

swing signal and the type of full swing signal. The phase-interpolation of the

non-full swing signal type generally employs the V-to-I current adder. The middle

phase can be generated by adding two signals with two different phases. A set of

binary code or temperature code is applied to control the tail current of the circuit

5   and to rectify the weighting of the adding signals. As a result, the phase of the

interpolation produced can be controlled to drift backward or forward. The

distribution of the phase is not distributed in one clock-pulse period uniformly

because the phase of the interpolation of the analog signal is decided by the

rating of the tail current of the current adder. The switch of the phase boundary is

10   non-seamless. We have to get the analog signal near the position of the

voltage-controlled oscillator for the phase interpolation because the input clock

signal is non-full swing signal. The result above will limit the application of the

data-recovery system of the multi-receiving channel described above. The phase

interpolation of the full swing signal will provide fewer globe clock signals of the

15   phase to produce near local multiphase clock. The characteristic above is the

advantage of the full swing signal type.

[0007]   The disadvantages of the phase-interpolation method in the type of

conventional full swing signal type include: (a) The decaying power of the

short-circuit current is large. (b) The nonlinear phase distribution. (c) The duty

20   cycle of the clock-pulse output is not 50%. The phase-interpolation circuit of the

full swing signal type in prior art is composed of two inverters 11 and 12 as which

shown in Fig. 1A. And the inverters are composed of the CMOS devices, as

which illustrated in Fig. 1B. The principle of the operation of the devices is to provide two-level clock signals CK1 and CK2. As shown in Fig. 1C, the phase of CK1 is before the phase of CK2 in order to produce an output signal with middle phase by short-circuit of the two inverters. However, as indicated by the arrow

5   shown in Fig. 1B, the circuit will produce a short-circuit current Isc when the time is T1 and T2 and when the   clock signal CK1 is in the input end 111 and the clock signal CK2 is in the input end 121. The disadvantage of large decaying power in the circuit exists. And the phase of the interpolation signal produced cannot be controlled in the middle range of the phase of the original signals.

10   [0008]   Please refer to Fig.1D which is a schematic diagram illustrating an improved prior art circuit employing the above mentioned method. The circuit shown in Fig.1D can correct the defects of the phase of the interpolation signal to be in the middle of the two original phases by fine tuning the current ratio of both discharging paths (e.g., to control the ratio of tail current). However, such kind of

15   method can only improve the linearity of the distribution of the phase by means of the ratio of current (e.g., W and 1-W shown in Fig.1D), which is difficult to be controlled concisely. This method cannot achieve the yield of the mass production and cannot maintain the duty cycle of the original clock-pulse. It will require an additional duty cycle correction circuit to maintain the 50% duty cycle.

20   [0009]   Fig. 2A describes another prior art circuit, in which a phase-interpolation circuit that can avoid short-circuit current is provided. However, it also incurs the

drawback of being only able to produce the interpolation phase for the falling

edge of the clock pulse, but cannot provide the interpolation phase for both the

rising and falling edges of the clock pulse (as which shown in Fig. 2B). Therefore,

such kind of circuit can only be used for doubling the frequency of multiphase

5   clock pulse. And it will not produce a new middle phase for the doubled frequency.

The primary object of the present invention is to improve the deficiencies of the

above mentioned conventional phase-interpolation circuits. The following

description is going to disclose a novel phase-interpolation circuit which can

avoid short-circuit current, provide linearly distributed multiphase clock pulse, and

10   maintain 50% duty cycle constantly. In addition, by applying the novel

phase-interpolation circuit of the present invention, we don't have to design

additional duty cycle correction circuit. Moreover, we will be able to interpolate

new middle phase between both the rising and falling edges of the clock pulse for

the full swing signal type (digital type) phase-interpolation circuit.

15   Summary of the Invention

[0010]   It is one of the object of the present invention is to provide a

phase-interpolation circuit which can avoid short-circuit current and generate

linearly distributed phase-interpolation signals.

[0011]   The phase-interpolation circuit disclosed to the embodiment of the

20   present invention comprises: a first inverter for receiving the first clock signal; a

second inverter for receiving the second clock signal, wherein an output end of

the second inverter is coupled to an output end of the first inverter to form a

common output end to output the third clock signal; a first controlled switch

coupled to the first inverter, the second inverter, and a power source, wherein the

5   first controlled switch being "off" when the first clock signal is in a fist state, and

being "on" when the first clock signal is in a second state; and a second

controlled switch coupled to the first inverter, the second inverter, and ground,

wherein the second controlled switch being "on" when the first clock signal is in

the first state, and being "off" when the first clock signal is in the second state.

10   The phase of the third clock signal is determined by the phase of the first clock

signal and the second clock signal and the first controlled switch and the second

controlled switch are to avoid a short-circuit current of the phase-interpolation

circuit.

[0012]   These and other objectives of the claimed invention will no doubt

15   become obvious to those of ordinary skill in the art after reading the following

detailed description of the preferred embodiment that is illustrated in the various

figures and drawings.

Brief Description of the Drawings

[0013]   Fig.1A is a schematic diagram of the first example of the conventional

20   phase-interpolation circuit of full swing signal type (digital type).

[0014]   Fig.1B is a schematic diagram showing the second example of conventional phase-interpolation circuit including inverters composed of the CMOS.

[0015]   Fig.1C is a schematic diagram showing the waveform of the   clock signals CK1 and CK2 provided by a conventional input phase-interpolation circuit.

[0016]   Fig.1D is a schematic diagram showing the third example of conventional phase-interpolation circuit.

[0017]   Fig.2A is a schematic diagram showing the forth example of conventional phase-interpolation circuit to avoid short-circuit current.

[0018]   Fig.2B is a schematic diagram showing the waveform of the conventional phase-interpolation circuit shown in Fig.2A.

[0019]   Fig.3 illustrates a schematic diagram of a preferred embodiment of the phase-interpolation circuit of the present invention.

[0020]   Fig.4A and Fig.4B illustrate two examples for using MOS to accomplish the controlled switch circuit disclosed in the embodiment of the present invention.

[0021]   Fig.5 is a schematic diagram illustrating the waveform including the clock signal CK1-2 outputted by the phase-interpolation circuit and the   clock

signal CK1 inputted in the phase-interpolation circuit.

[0022]   Fig.6 is a schematic diagram illustrating a preferred embodiment of the phase-interpolation signal generating device of the present invention.

[0023]   Fig.7A, Fig.7B, Fig.7C and Fig.7D and Fig.7E are schematic diagrams

5   showing the waveform in different clock-pulse signals generated by the device shown in Fig.6.

[0024]   Fig.8 is a schematic diagram illustrating another preferred embodiment of the phase-interpolation signal generating device of the present invention which can generate eight output multiphase signals based on four input multiphase

10   signals.

Detailed Description of the Preferred Embodiments

[0025]   Please refer to Fig.3, which is a schematic diagram of a preferred embodiment of the phase-interpolation circuit of the present invention. The phase-interpolation circuit shown in Fig.3 includes five inverters and two

15   controlled switches. The input end 311 of the first inverter 31 receives a phase-leading   clock signal CK1. And the input end 321 of the second inverter 32 receives a phase-following   clock signal CK2. And the output end 322 of the second inverter 32 is connected to the output end 312 of the first inverter 31 to

form a common output end 30. The input end 331 of the third inverter 33

connects to the common output end 30 electrically. The output ends of the fourth

inverter 36 and the fifth inverter 37 are connected to the input ends of the first

inverter 31 and the second inverter 32 respectively.

5   [0026]   The circuit further includes the first controlled switch 34 and the second

controlled switch 35 to avoid short-circuit current in the present invention. The

first controlled switch 34 connects between the first inverter 31 and the second

inverter 32 and the electrical power source (VDD). The switch 34 is off when the

clock signal CK1 is in the high-level state. The switch 34 will be turn on when the

10   clock signal CK1 is in the low-level state. The second controlled switch 35

connects between the first inverter 31 and the second inverter 32 and the ground

(GND) electrically. The second controlled switch 35 is on when the   clock signal

CK1 is in the high-level state. And the second controlled switch 35 is off when the

clock signal CK1 is in the low-level state. By controlling the timing of the

15   open/close states of the controlled switches 34 and 35 with the   clock signal

CK1, short-circuit current can be omitted.

[0027]   Please refer to Fig.4A and Fig.4B. The inverter shown in Fig.4A and

Fig.4B is composed of CMOS inverters. In the following description, we will let "1"

represent the high-level state and let "0" represent the low-level state for

20   illustration convenience. When the state of (CK1,CK1) is changing from (0,0) to

(1,0) to (1,1), and when CK1 rises from "0" to "1", the clock signal CK2 will also

rise from "0" after then. In the same time, the common output end 30 is going to fall from "1" to "0". The PMOS in the controlled switch will be off and the NMOS in the controlled switch will be on when CK1="1". Because the VDD is disconnected now, therefore the short-circuit current will not be generated even when the

5   NMOS of the first inverter 31 is on and the PMOS of the second inverter 32 is on to form a short-circuit path and when (CK1,CK2) is equal to (1,0). The function of the common output end 30 also matches the need of phase-interpolation since the dispersion capacitor thereof will discharge to "0" gradually. Vice versa, when (CK1,CK2) is changing from (1,1)-(0,1)-(0,0). The clock signal CK2 will fall down

10   from "1" after the CK1 fall down to "0". In the same time, the common output end will rise from "0" to "1". The PMOS will be on and the NMOS will be off when CK1="0". Because the connection toward GND is off now, therefore the short-circuit current will not be generated even when (CK1,CK2) is equal to (0,1) and the PMOS of the first inverter 31 and the NMOS of the second inverter 32

15   are both on to form a short-circuit path there between. And the common output end 30 matches the need of the phase-interpolation function because the dispersion capacitor will charge to "1" gradually. The signal comes from the common output end 30 will be further processed by the third inverter 33 so as to output the wave forms shown in Fig.5. In which, the output clock signal CK1-2

20   is right between CK1 and CK2. The electric power decay can be minimized in the present invention because we effectively avoid the short-circuit current.

[0028]   However, since the middle phase signal is generated by the

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charging/discharging processes of the capacitors of different inverters controlled by different clock pulses with different phases, therefore the middle phase signal might drift toward one of the neighbor phases (e.g., P1 is unequal to P2 in Fig.5) if the charging/discharging speed or ratio is improper or not precisely controlled.

5   As a result, the 50% duty cycle may drift. Although the error of the middle phase might be smaller than 3% if suitable parameters are adjusted, however, many uncertainties such like changing of temperature, manufacturing error and dispersion capacitors may still make the middle phase to drift away from the ideal value.

10   [0029]   To resolve this problem, the present invention discloses a phase-interpolation generated device as shown in Fig.6. The device comprises five phase-interpolation circuits. Each phase-interpolation circuit can be accomplished by using the circuit illustrated in Fig.3. These five phase-interpolation circuits include the first phase-interpolation circuit 61, the

15   second phase-interpolation circuit 62, the third phase-interpolation circuit 63, the fourth phase-interpolation circuit 64 and the fifth phase-interpolation circuit 65. The both input ends of the first phase-interpolation circuit 61 are connected to receive the first   clock signal CK0. And the two input ends of the second phase-interpolation circuit 62 are separately directed to receive the first   clock

20   signal CK0 and the second   clock signal CK1 respectively. And the both input ends of the third phase-interpolation circuit 63 receive the second   clock signal CK1. And the two input ends of the fourth phase-interpolation circuit 64 are

separately connected to the output ends of the first phase-interpolation circuit 61

and the second phase-interpolation circuit 62 respectively. And the output end of

the fourth phase-interpolation circuit 64 will output the third   clock signal CK2-0.

The two input ends of the fifth phase-interpolation circuit 65 are respectively

5   connected to the output ends of the second phase-interpolation circuit 62 and the

third phase-interpolation circuit 63. And the output end of the fifth

phase-interpolation circuit 65 outputs the fourth   clock signal CK2-1.

[0030]   The wave forms shown in Fig.7A schematically illustrate an example of

the first   clock signal CK0 and the second   clock signal CK1. The Fig.7B

10   illustrates the signal of the common output end 30 of the first-stage

phase-interpolation circuit. For some uncertainties as mentioned above, the

middle phase might drift as shown in Fig.7B. The middle phase obtained after the

process of the third inverter 33 is shown in Fig.7C. The schematics of the signal

of the common output end 30 in the second-stage phase-interpolation circuit

15   connected is shown in Fig.7D. Because the clock pulse is processed by two

stages of same phase-interpolation circuits, the leading and following clock

pulses are in the same process of the leading and following paths. In addition,

the interpolation of the phases is also facing the same process of the

phase-interpolation of the rising and falling edges. Therefore, unbalance of the

20   NMOS and PMOS as well as other uncertain effects can be averaged to

compensate the non-linearity of the phase distribution. As shown in Fig.7E, the

output wave forms of the third   clock signal CK2-0 and the fourth   clock signal

CK2-1 will have phases uniformly distributed in a period of clock pulse. Experimental simulation indicates that the error of the linear distribution of the phase will be smaller than 0.1%. The signal is processed in the rising and falling edges of the phase-interpolation circuit which corrects the 50% duty cycle of the

5   output clock pulse because of the characteristics of the phase-interpolation of the inversion. Experimental simulation indicates that the error of the duty cycle will be smaller than 1% and will not be influenced by aforementioned uncertainties. We can improve the linearity of the phase and the 50% duty cycle of the phase-interpolation distribution after the phase-interpolation module and the

10   phase averaging module. Applications for the novel circuit disclosed in the present invention will be improved vastly.

[0031]   Fig.8 is a schematic diagram illustrating another preferred embodiment of the phase-interpolation signal generating device of the present invention which can   generate eight output multiphase signals (CK0~CK7 of the output ends)

15   based on four input multiphase signals (CK0~CK3 of the input ends).

[0032]   While the present invention has been shown and described with reference to a preferred embodiment thereof, and in terms of the illustrative drawings, it should be not considered as limited thereby. Various possible modification, omission, and alterations could be conceived of by one skilled in the

20   art to the form and the content of any particular embodiment without departing from the scope and the spirit of the present invention.